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Design Review

Designing an Efficient Sub-threshold FPGA Switchbox

**Completed tasks**

So far, we’ve been able to create a simulation in cadence that shows (in a simplified sense) the interconnect between two Configurable Logic Blocks (CLBs) in a Field Programmable Gate Array (FPGA). The simulation schematic consists of a buffered input signal (which represents the signal that would come from a CLB) that travels through a segment of then through a switchbox, then through another segment of wire and a second switchbox, and repeats until the signal reaches the last wire (which represents the signal reaching the destination CLB). In our initial schematic, we include 20 switch boxes, and we measure the output signal after 2, 4, 10, and 20 switchboxes. Our simulation results showed a nearly perfect linear relationship between number of switchboxes and delay, illustrating the need to minimize the number of switchboxes between CLBs in a FPGA.

In terms of the switchboxes, we’ve explored two types of switches: tri-state buffers (TSBs) and transmission gates (TXs). From our initial simulations of transmission gates, we’ve run into multiple issues. The simulation results show very weird phenomena,, and we are sure that this is not how transmission gates in FPGA fabric work. We will include the resulting waveforms, but we understand that there are major issues with the response we have generated. We will take the time to sort through these issues before the proposal.

**Tasks prior to proposal**

Making simulations more characteristic of Sub-VT FPGA

The current simulations that we have done used approximations for wire length, wire resistance, and wire capacitance found in a paper that we reviewed [*see Summary 4*]. That paper assumed 0.13 µm technology, but what we want to simulate is 90 nm technology. Thus, the values for resistance and capacitance that we have used thus far are more than likely not characteristic of 90 nm technology. Further investigation is required to find more characteristic values for typical wire lengths, resistance, and capacitance.

Broadening Simulations to include more knobs and metrics

Before we can truly begin to explore a design to minimize power and area, we need to see how other factors affect the performance of our switchboxes. Currently, we have only tested one independent variable, the number of switchboxes. There are numerous other factors to consider. Here are some of them:

* Signal speed – How the switchbox delay and voltage swing changes with different frequency signals
* Signal voltage – How the switchbox delay and voltage swing change with a larger/smaller input voltage swing. This is especially important, because we final goal is to delve into the sub-threshold region.
* Number of Wire Segments – Dividing the wires into more segments increases the Elmore delay, which can increase the overall delay. We will need to determine how to divide the wire to have the most accurate simulation
* Length of Wire – So far we have been keeping the length of wire constant, but it is clear that in a FPGA, paths can have different lengths. We will need to do simulations in order to see if how different switchbox designs respond to different wire lengths

We also need to increase the number of metrics we are keeping track of. Originally, we were only concerned with propagation delay, but there are other factors that will be important to minimize/maximize in our design. These metrics include the total area, or number of transistors, voltage swing degradation, and voltage overhead, which corresponds directly to power dissipation.

**Tasks Still to be done (After proposal)**

Once we have a better understanding of how the switchboxes in FPGAs respond to the different parameters of the test circuit, we can begin to think about and eventually design a new FPGA switchbox that will ideally minimize power dissipation and area while maintaining signal fidelity. This new design may include tri-state buffers and transmission gates, and it may have completely different structures included. Running more simulations and seeing more of the response to changing parameters will give us more insight into the functionality of the switchbox, and help us to come up with a solution to the problem.

Upon the completion of the design, we will then run simulations with the design and compare the results with the current design models we simulated earlier, after which we will know whether or not the new design truly meets our requirements.